BUK7675-55A

N-channel TrenchMOS standard level FET

25 August 2014 **Product data sheet**

1. General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

2. Features and benefits

- AEC Q101 compliant
- Low conduction losses due to low on-state resistance
- Suitable for standard level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

3. Applications

- 12 V and 24 V loads
- Automotive and general purpose power switching
- Motors, lamps and solenoids

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	-	55	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2; Fig. 3		-	-	20.3	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	62	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A; T_j = 175 °C; Fig. 11; Fig. 12		-	-	150	mΩ
		V_{GS} = 10 V; I_D = 10 A; T_j = 25 °C; Fig. 11; Fig. 12		-	64	75	mΩ
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 11 A; $V_{sup} \leq 55$ V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped		-	-	30.3	mJ

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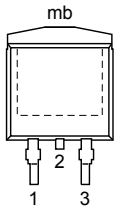
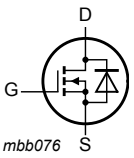
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 D2PAK (SOT404)	
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7675-55A	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7675-55A	BUK7675-55A

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	55	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 kΩ		-	55	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	62	W
I_D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; Fig. 2; Fig. 3		-	20.3	A
		T_{mb} = 100 °C; V_{GS} = 10 V; Fig. 2		-	14.3	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \leq 10$ µs; Fig. 3		-	81	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C

Symbol	Parameter	Conditions		Min	Max	Unit
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	20.3	A
I_{SM}	peak source current	pulsed; $t_p \leq 10$ µs; T_{mb} = 25 °C		-	81	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 11 A; $V_{sup} \leq 55$ V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped		-	30.3	mJ

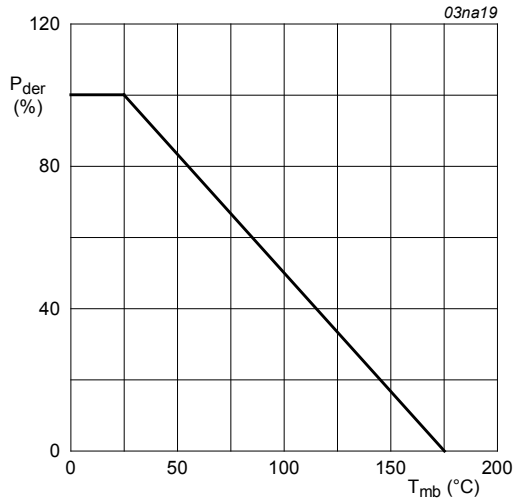


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

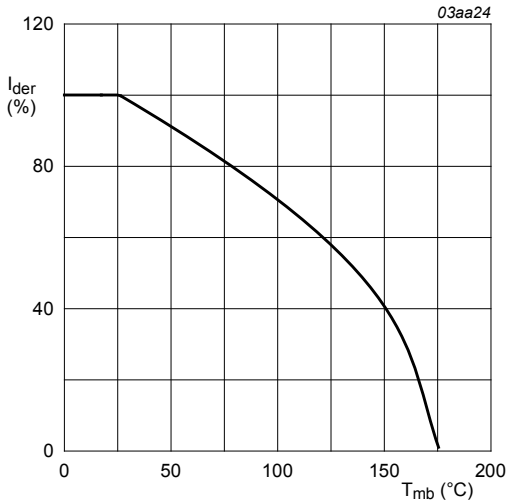


Fig. 2. Normalized continuous drain current as a function of mounting base temperature

$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\,\%$$

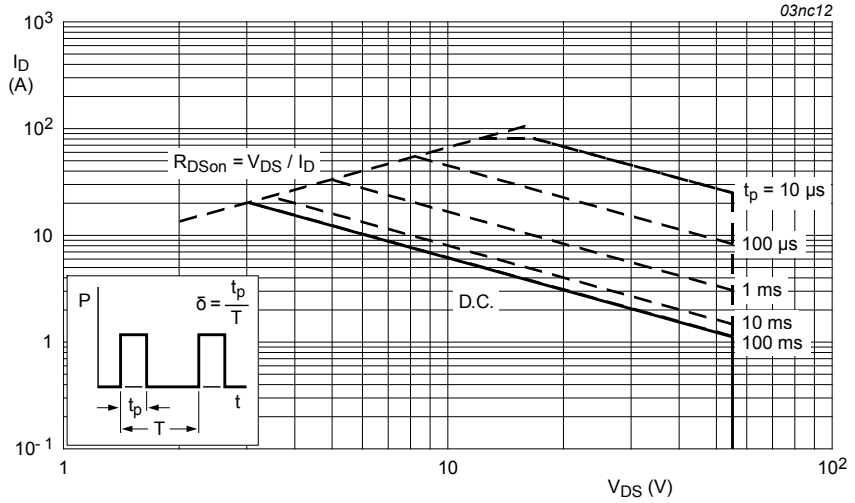


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$$T_{mb} = 25°C; I_{DM} \text{is single pulse}$$

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4		-	-	2.4	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on printed-circuit board; minimum footprint		-	50	-	K/W

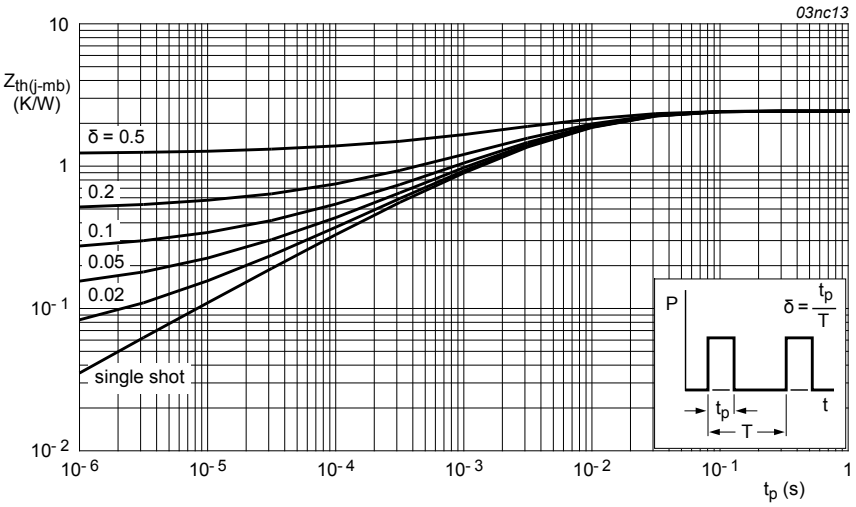


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V; T_j = 25 °C		55	-	-	V
		I_D = 0.25 mA; V_{GS} = 0 V; T_j = -55 °C		50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; Fig. 10		1	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; Fig. 10		2	3	4	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; Fig. 10		-	-	4.4	V
I_{DSS}	drain leakage current	V_{DS} = 55 V; V_{GS} = 0 V; T_j = 175 °C		-	-	500	µA
		V_{DS} = 55 V; V_{GS} = 0 V; T_j = 25 °C		-	0.05	10	µA

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A; T_j = 175 °C; Fig. 11; Fig. 12		-	-	150	mΩ
		V_{GS} = 10 V; I_D = 10 A; T_j = 25 °C; Fig. 11; Fig. 12		-	64	75	mΩ
Dynamic characteristics							
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C; Fig. 13		-	320	483	pF
C_{oss}	output capacitance			-	92	113	pF
C_{rss}	reverse transfer capacitance			-	64	90	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 10 Ω; T_j = 25 °C		-	10	-	ns
t_r	rise time			-	50	-	ns
$t_{d(off)}$	turn-off delay time			-	70	-	ns
t_f	fall time			-	40	-	ns
L_D	internal drain inductance	from upper edge of drain mounting base to centre of die; T_j = 25 °C		-	2.5	-	nH
		from drain lead 6 mm from package to centre of die; T_j = 25 °C		-	4.5	-	nH
L_S	internal source inductance	from source lead to source bond pad; T_j = 25 °C		-	7.5	-	nH
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 15 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 14		-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = -10 V; V_{DS} = 30 V; T_j = 25 °C		-	32	-	ns
Q_r	recovered charge			-	120	-	nC

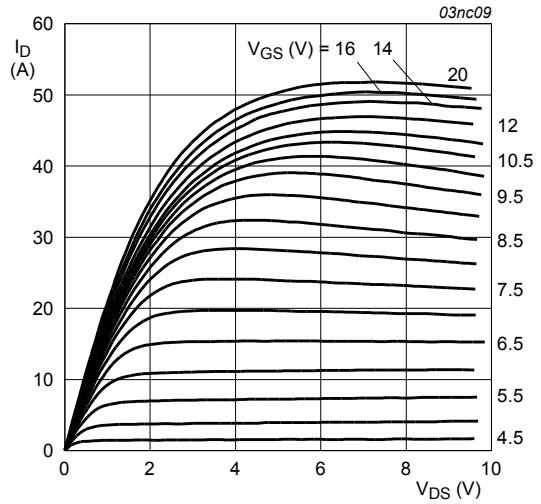


Fig. 5. Output characteristics; drain current as a function of drain-source voltage; typical values

$T_j = 25°C$

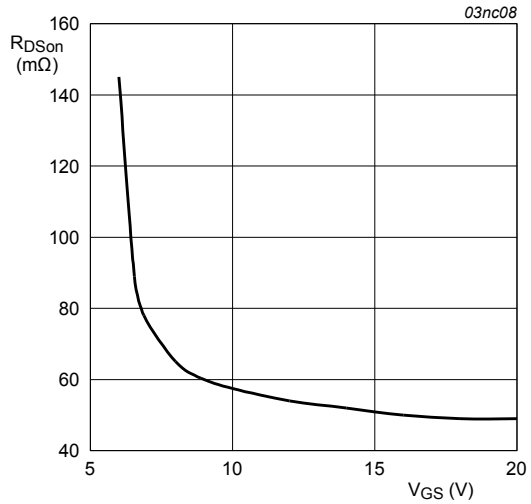


Fig. 6. Drain-source on-state risistance as a function of gate-source voltage; typical values

$T_j = 25°C; I_D = 10A$

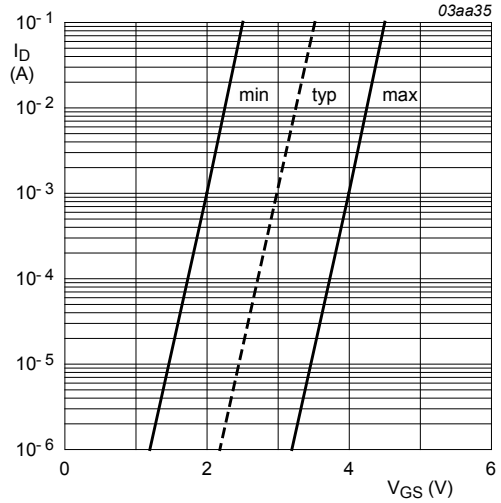


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25\,°C; V_{DS} = 5V$

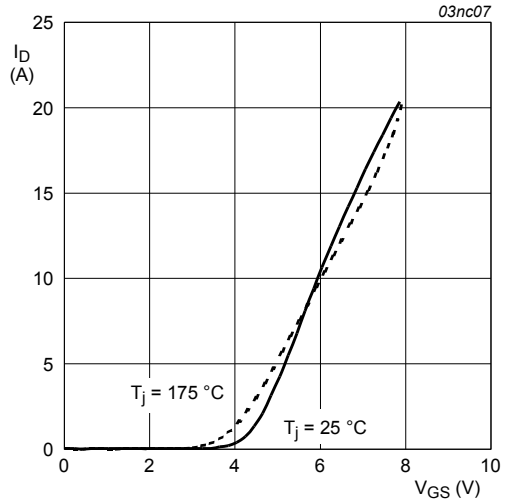


Fig. 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$V_{DS} = 25V$

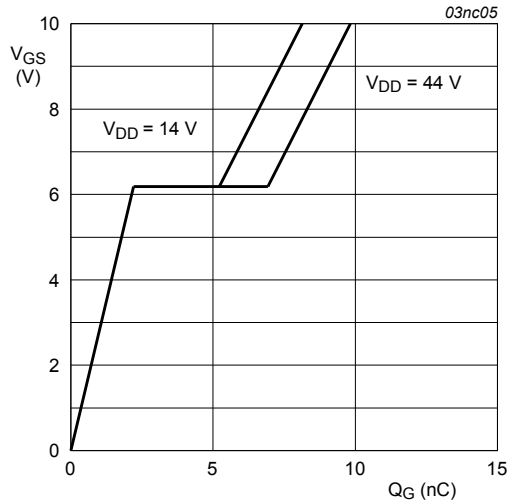


Fig. 9. Gate-source voltage as a function of gate charge; typical values

$T_j = 25°C; I_D = 10A$

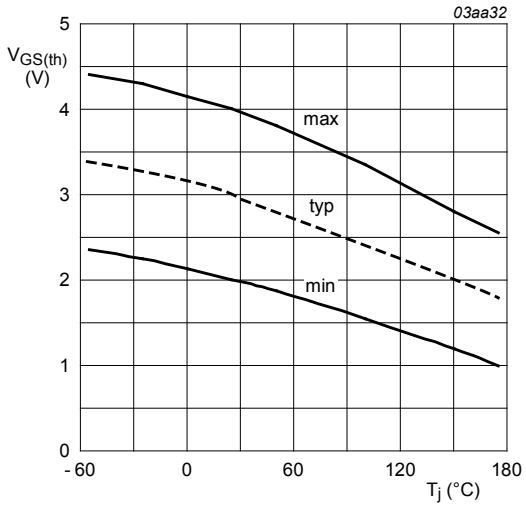


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$I_D = 1mA; V_{DS} = V_{GS}$

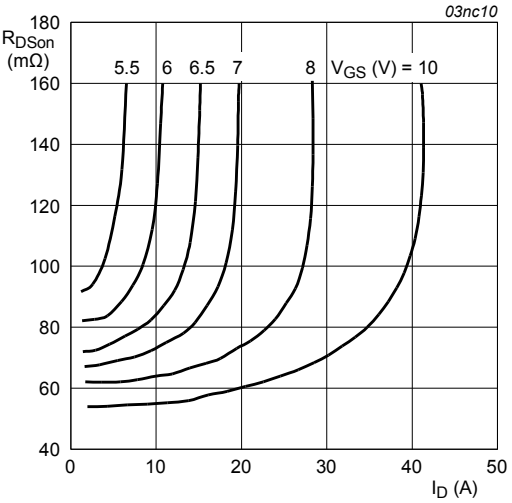


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25°C$

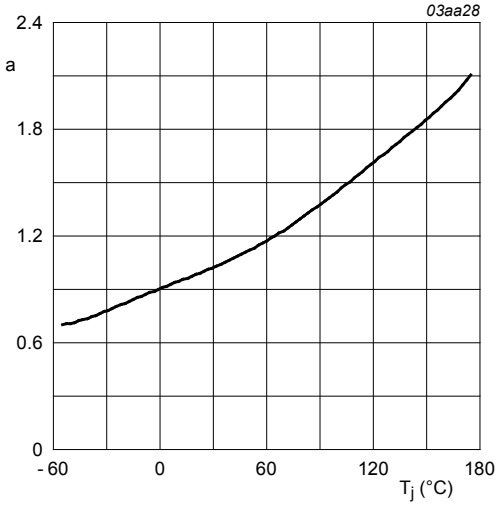


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

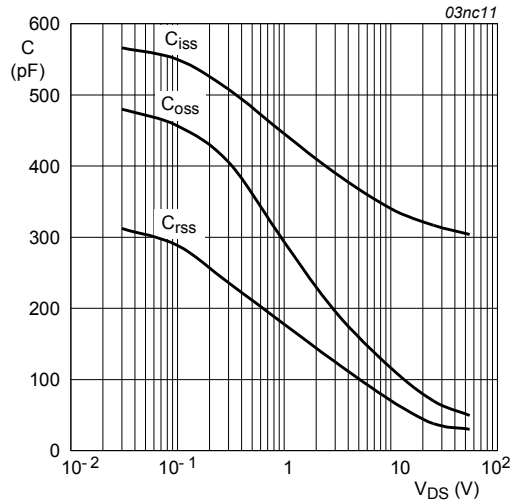


Fig. 13. Input, output and reverse capicitances as a function of drain-source voltage; typical values

$V_{GS} = 0V; f = 1MHz$

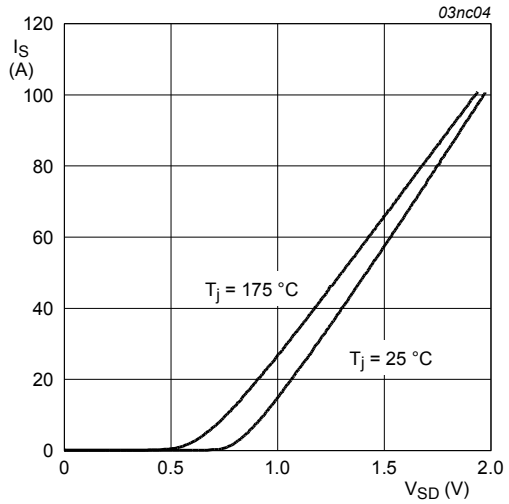
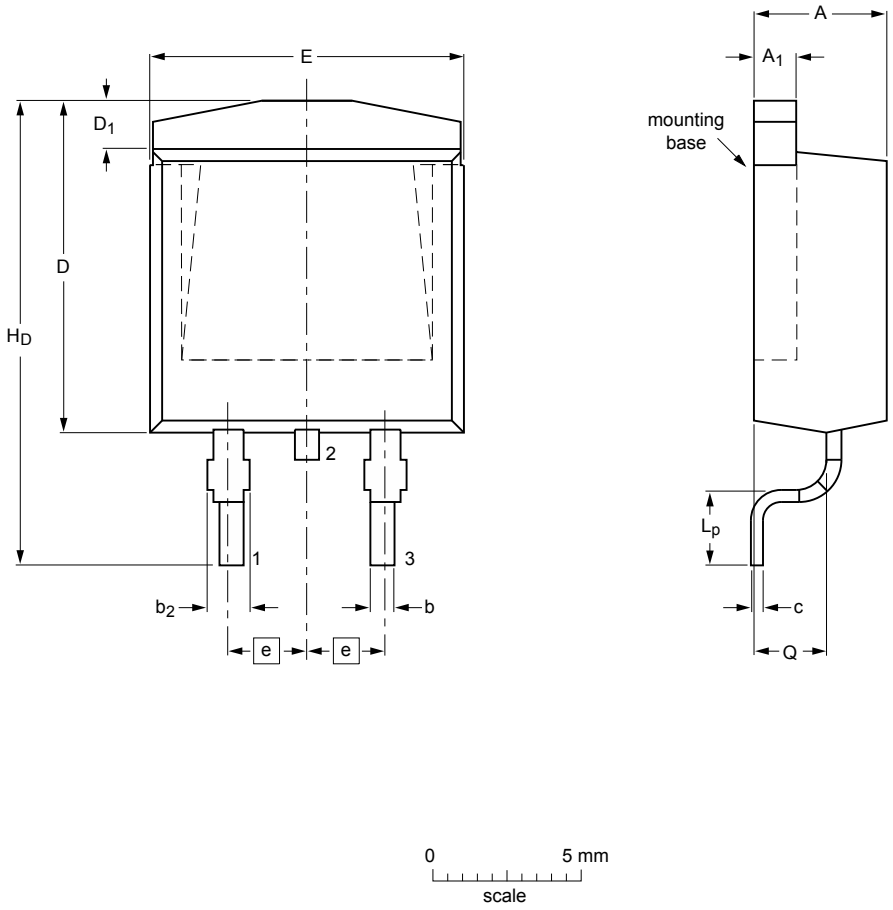


Fig. 14. Reverse diode current as a function of reverse dioode voltage; typical values

$V_{GS} = 0V$

11. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) **SOT404**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b	b_2	c	D	D_1	E	e	H_D	L_p	Q
mm	max	4.5	1.40	0.85	1.45	0.64	11	1.6	10.3		15.8	2.9	2.6
	nom									2.54			
	min	4.1	1.27	0.60	1.05	0.46		1.2	9.7		14.8	2.1	2.2

sot404_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT404						~~06-03-16~~ 13-02-25

Fig. 15. Package outline D2PAK (SOT404)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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